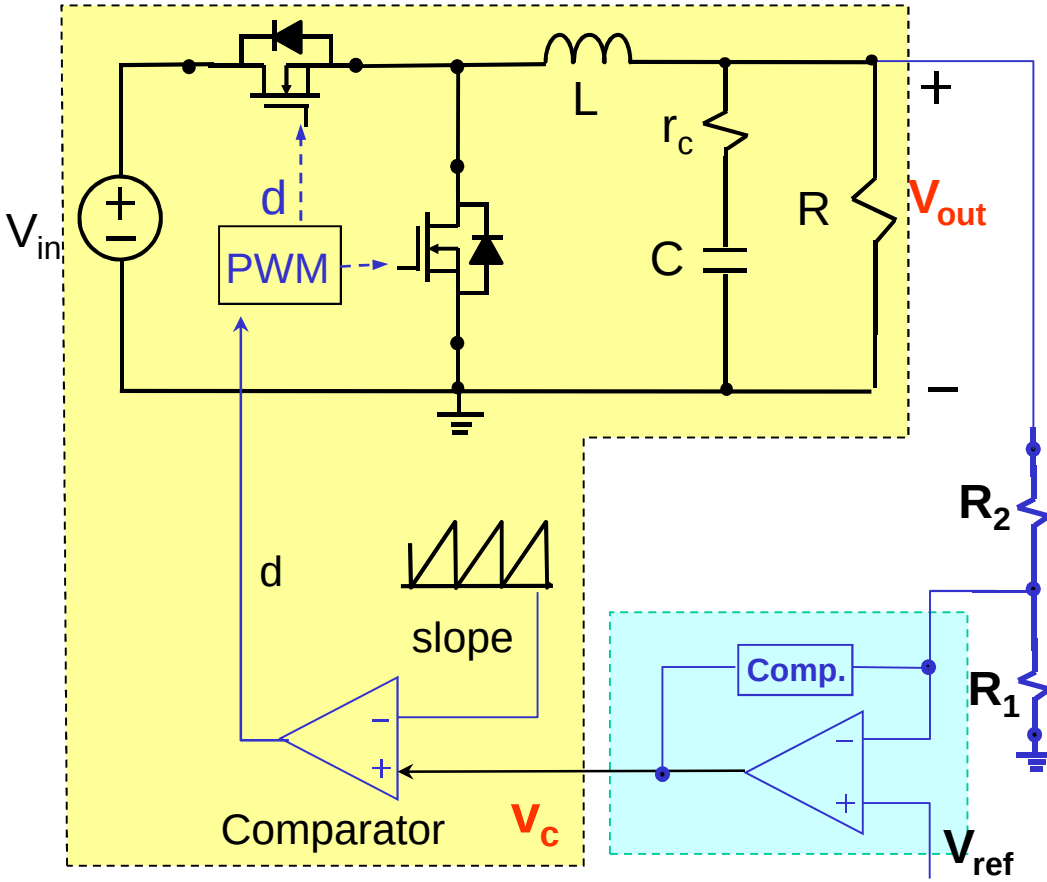
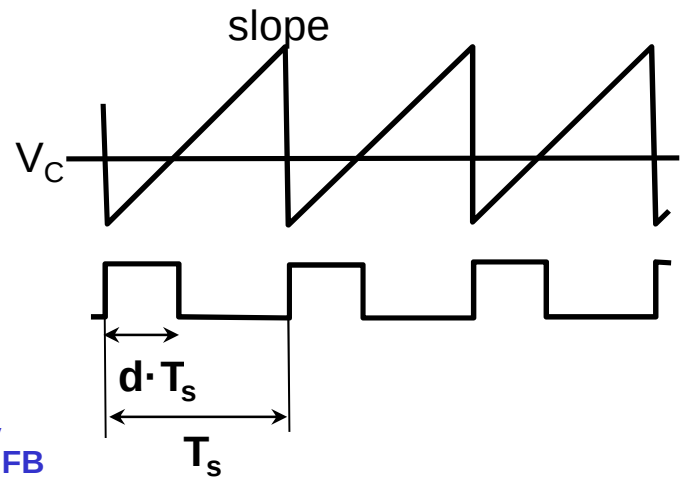
Loop Compensation Basics

Voltage-Mode Control Basics

Voltage-Mode Controlled Buck Converter



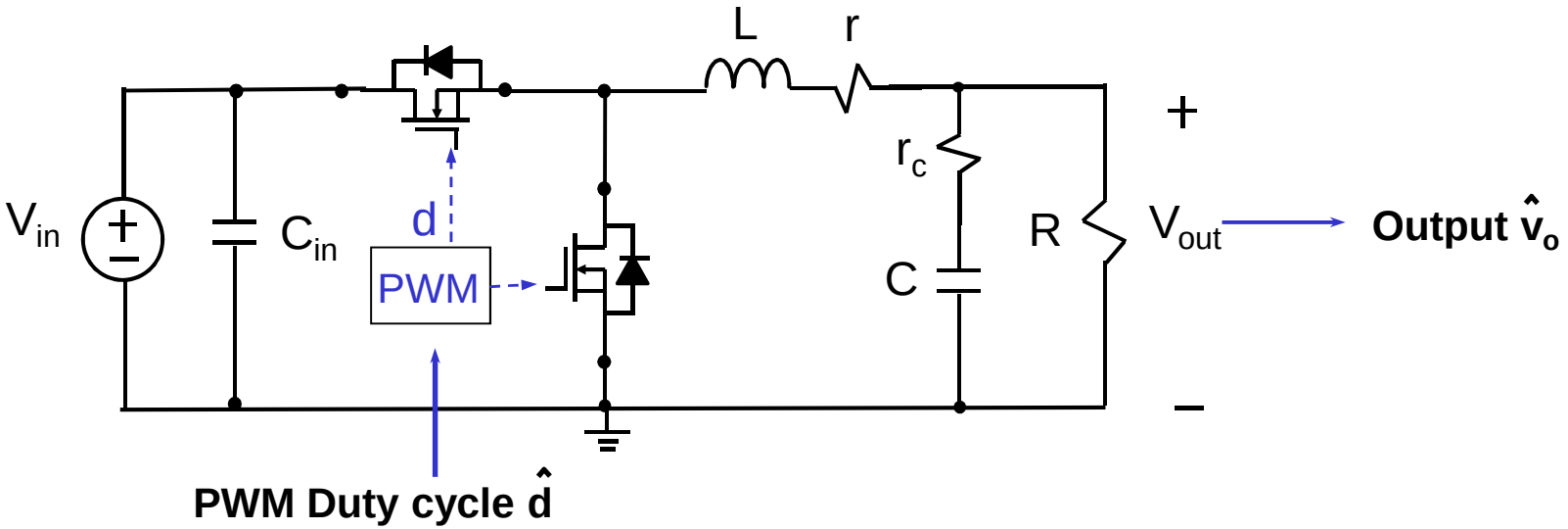


$d = k \cdot V_c$

Power Stage
Control-to-output

Error Op-Amp
Compensation A(s)

Buck Converter Power Stage Control-to-Output



Control-to-output transfer function:

$$G_{dv}(s)=\frac{\hat{v}_o}{\hat{d}}=\frac{V_{in}\cdot\left(1+\dfrac{s}{s_{z\_ESR}}\right)}{1+\dfrac{s}{\varpi_o\cdot Q}+\dfrac{s^2}{\varpi_o^2}}$$

ESR Zero:

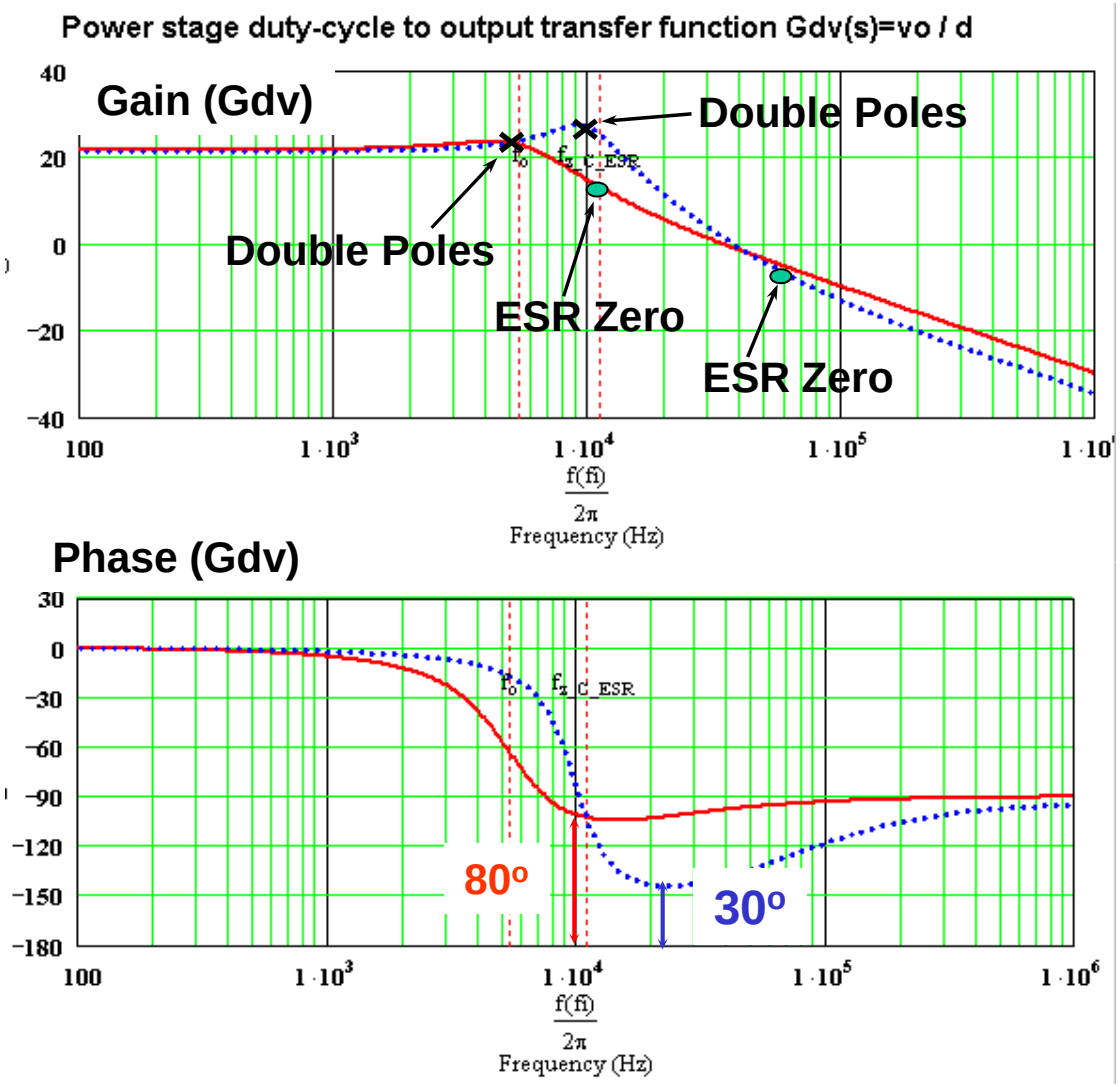
$$f_{Z\_ESR}=\frac{1}{2\pi}\cdot\frac{1}{r_C\cdot C}$$

Resonant double poles:

$$f_{o\_p}\approx\frac{1}{2\pi}\cdot\frac{1}{\sqrt{L\cdot C}}$$

- 1 zero, 2 poles system.

Buck Converter Control-to-Output Transfer Function



1 — **Reference design**
3X470uF Kemet Tantalum cap.
r_C=30mΩ

2 ····· **Customer design**
2 X 220uF Panasonic SP cap.
r_C=12mΩ

Double Poles: -180°
ESR Zero: +90°

Control loop is a strong function of output capacitor ESR

Voltage Loop Compensation Design

1. Select desired cross over frequency f_C

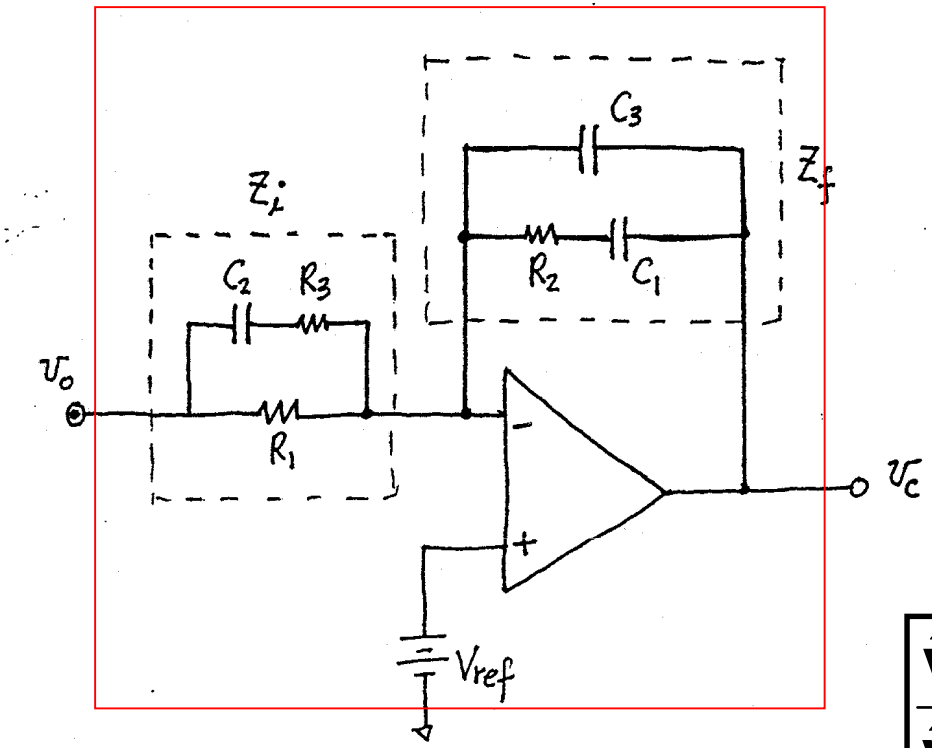
$$f_{C(\max)} = \frac{f_{SW}}{10} \sim \frac{f_{SW}}{5}$$

2. Loop compensation – type III compensation network

- One pole, low frequency integrator for high DC gain
- Two zeros located around L-C resonant double poles
- Two high-frequency poles:
  - to attenuate high frequency noise
  - to ensure the magnitude of the loop gain keeps decreasing after the 0dB crossover

Type III Compensation Network

(Typical 3-Pole, Two-Zero system in Voltage Mode Control)



$$\frac{\hat{v}_c}{\hat{v}_o} = -\frac{Z_f}{Z_i}$$

$$Z_i = R_1 // \left(\frac{1}{sC_2} + R_3 \right)$$

$$Z_f = \frac{1}{sC_3} // \left(\frac{1}{sC_1} + R_2 \right)$$

$$\frac{\hat{v}_c}{\hat{v}_o} = -\frac{\omega_I}{s} \frac{(1 + s/\omega_{Z1})(1 + s/\omega_{Z2})}{(1 + s/\omega_{P1})(1 + s/\omega_{P2})}$$

where:

$$\omega_{Z1} = \frac{1}{R_2 C_1}, \quad \omega_{Z2} = \frac{1}{C_2 (R_1 + R_3)}$$

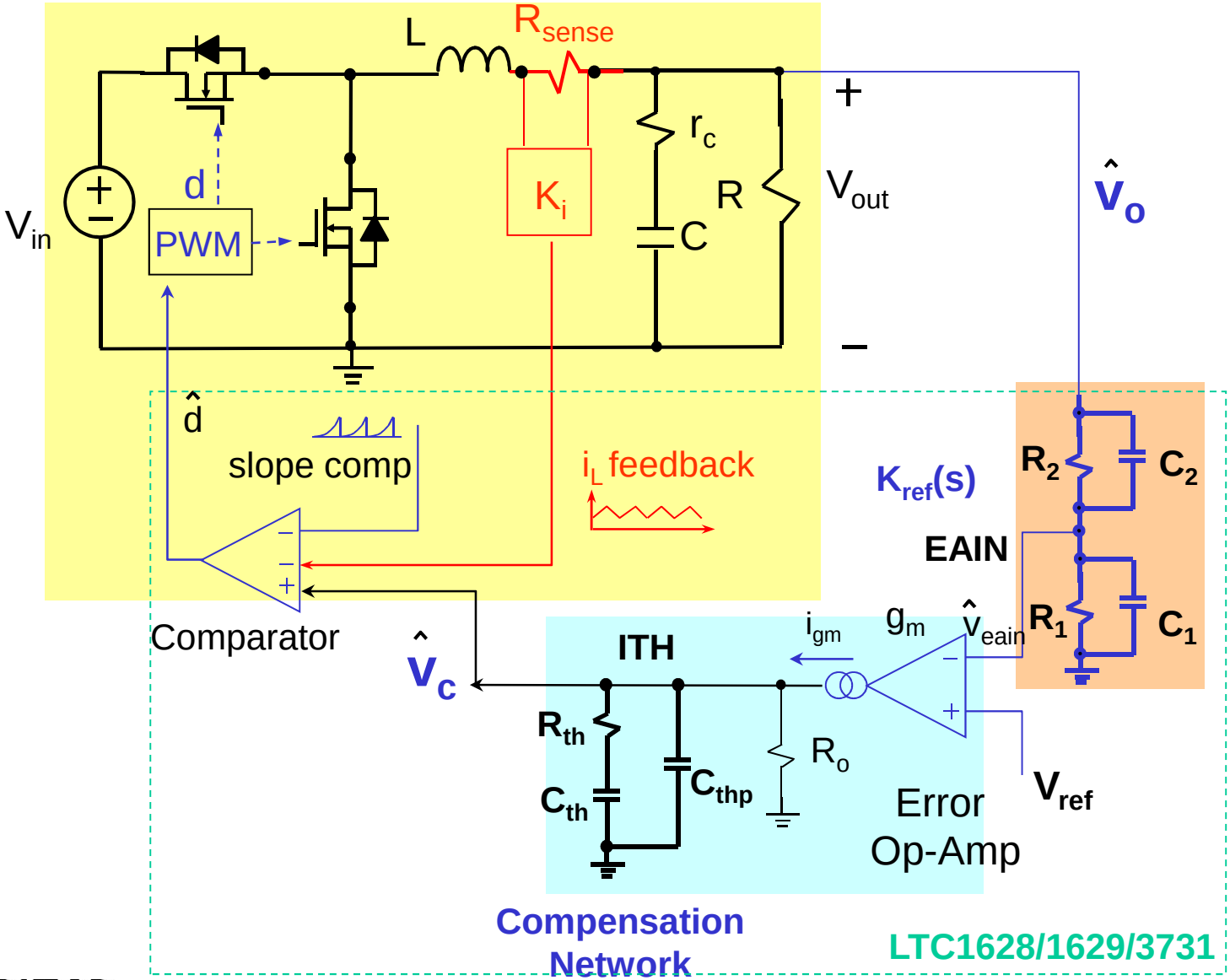
$$\omega_I = \frac{1}{R_1 (C_1 + C_3)} \qquad \omega_{P1} = \frac{1}{R_3 C_2}, \quad \omega_{P2} = \frac{1}{R_2 \cdot \frac{C_1 C_3}{C_1 + C_3}}$$

Pros and Cons of Voltage Mode Regulators

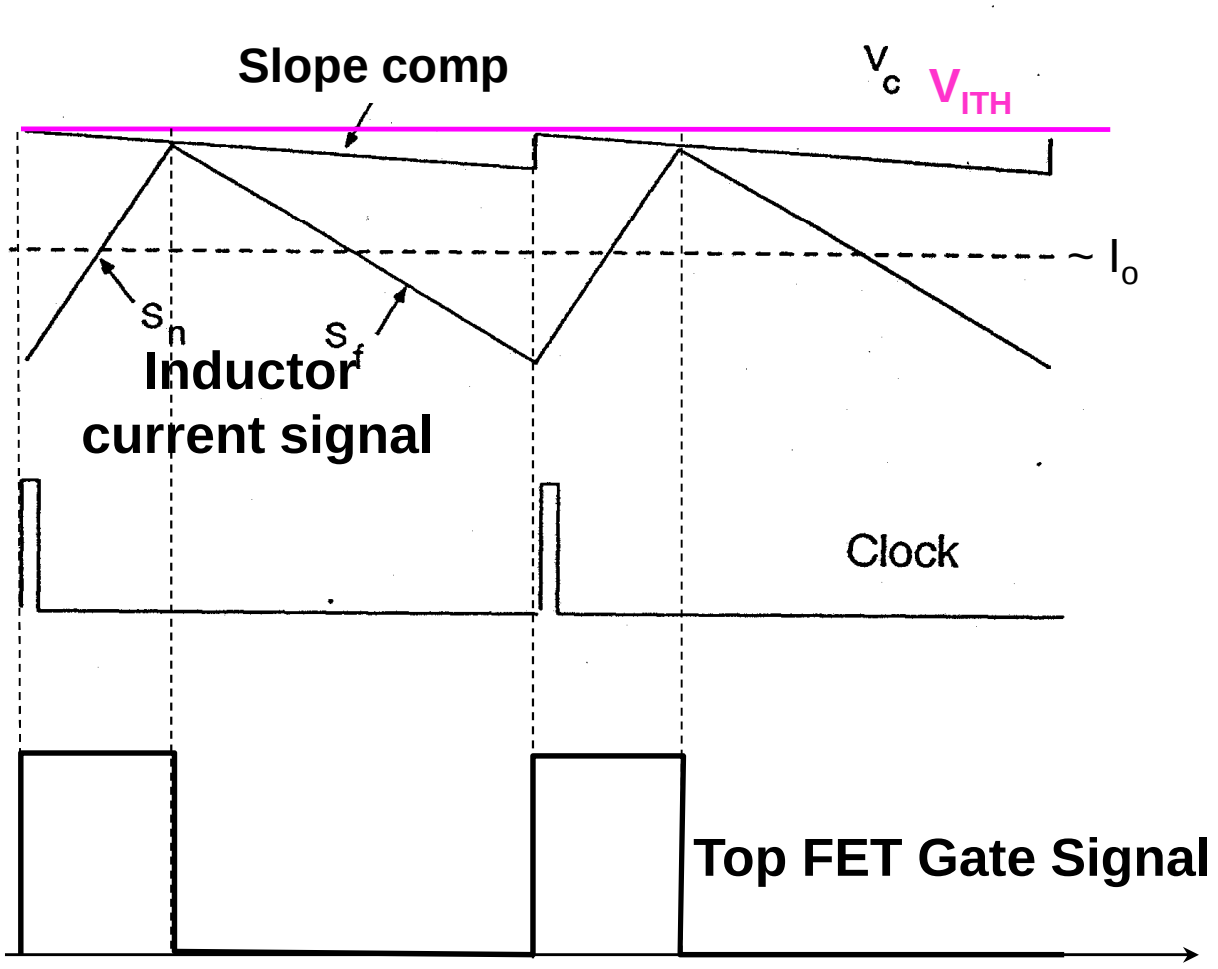
- **Pros:**
  - Don't need dedicated current sensing R : high efficiency and low cost solution
- **Cons:**
  - Loop gain is a function of Vin
    - Solution: Vin feed-forward compensation
  - Loop gain is a function of output ESR
    - Need carefully loop compensation design
  - Need to compensate for double resonant pole
  - The current sensing / limit is slow and not accurate
  - Need external loop for current sharing if two supplies / phases are in parallel

Current Mode Control Basics

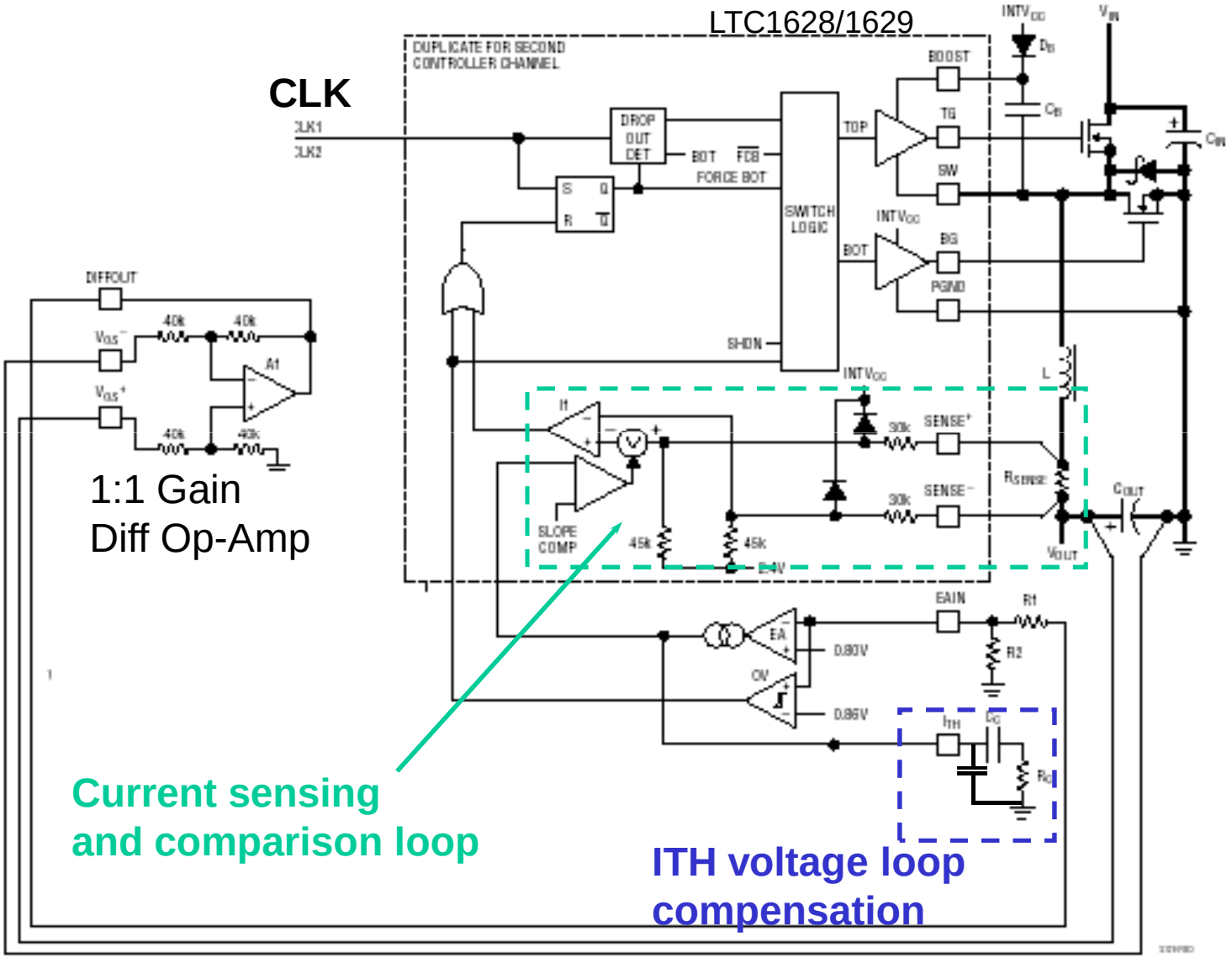
Simplified Block Diagram of Current Mode IC



Peak Current Mode Control

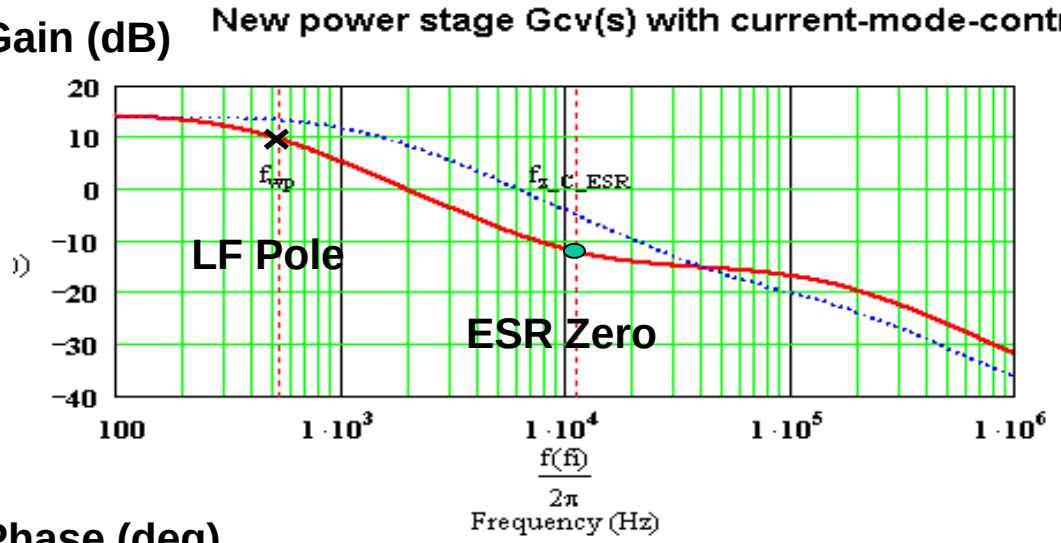


LTC's Current-Mode Controller Block Diagram

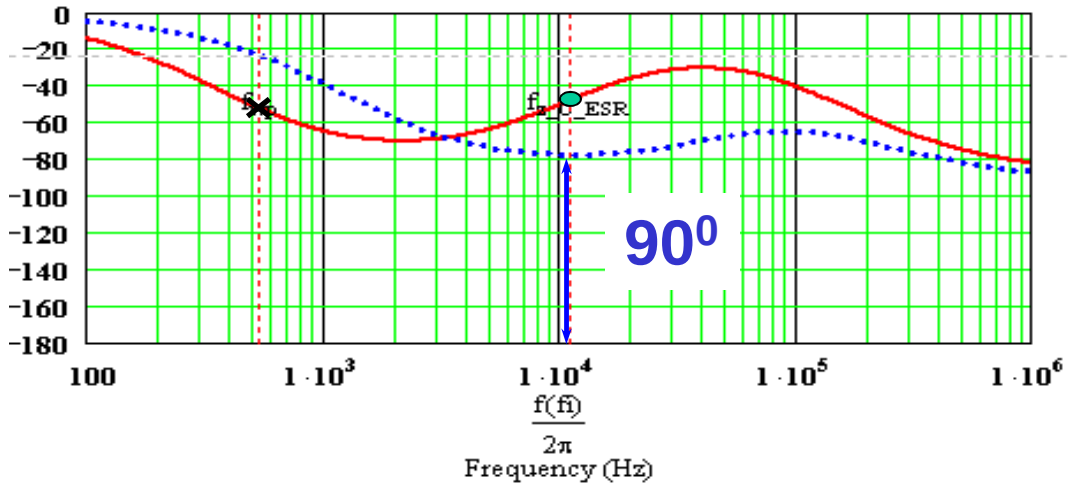


Power Stage Transfer Function With Closed Current Loop

Gain (dB)



Phase (deg)

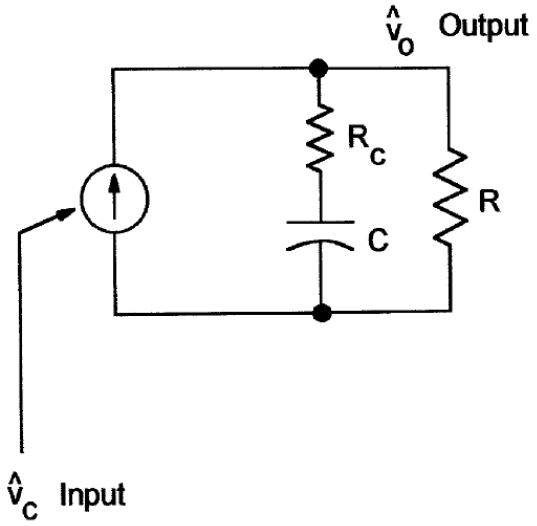


1 — **Reference design**
3X470uF Kemet cap.
r_C=30mΩ

2 ····· **Customer design**
2 X 220uF Panasonic cap.
r_C=12mΩ

- **Reduce phase delay with different output capacitors**
- **Stable system with reduced output capacitors / cost.**

Buck Converter Power Stage Control-to-Output



Simplest small-signal model : current source feeding the load

Low frequency model

Control-to-output transfer function:

$$G_{cv}(s) = \frac{\hat{v}_o}{\hat{v}_c} = K \frac{(1+\frac{s}{s_z})}{(1+\frac{s}{s_p})}$$

$$f_Z = \frac{1}{2\pi} \cdot \frac{1}{R_C \cdot C}$$

$$f_P = \frac{1}{2\pi} \cdot \frac{1}{R \cdot C}$$

- 1 zero, 1 pole system.

Pros and Cons of Current Mode Control

- **Pros:**
  - **Accurate / fast cycle-by-cycle current limit**
  - **True soft-start of inductor current**
  - **Easy to parallel phases / converters for high current**
  - **Accurate / fast current sharing**
  - **Very good line ripple rejection**
  - **Simple loop compensation with wide range of COUT, including Ceramic**
  - **High reliability**
- **Cons:**
  - **Need current sensing Rsense or RDSON, noise immunity**
  - **Subharmonic instability (ramp compensation)**
  - **Duty cycle limitation (ton, toff) due to current sensing delay**
  - **Higher output impedance at low frequency**

Loop Compensation Design
Of Current Mode Control

Voltage Loop Compensation Design

1. Select desired cross over frequency f_C

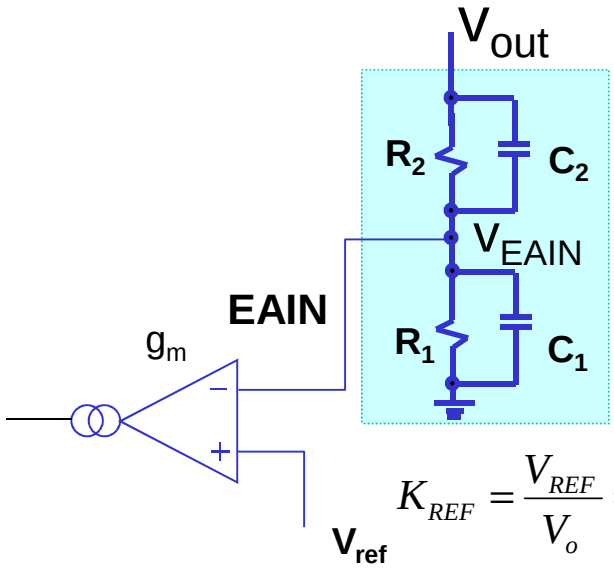
$$f_{C(\max)} = \frac{f_{SW}}{10} \sim \frac{f_{SW}}{5}$$

2. Choose desired loop phase margin:

Phase margin >= 45^o for buck converter

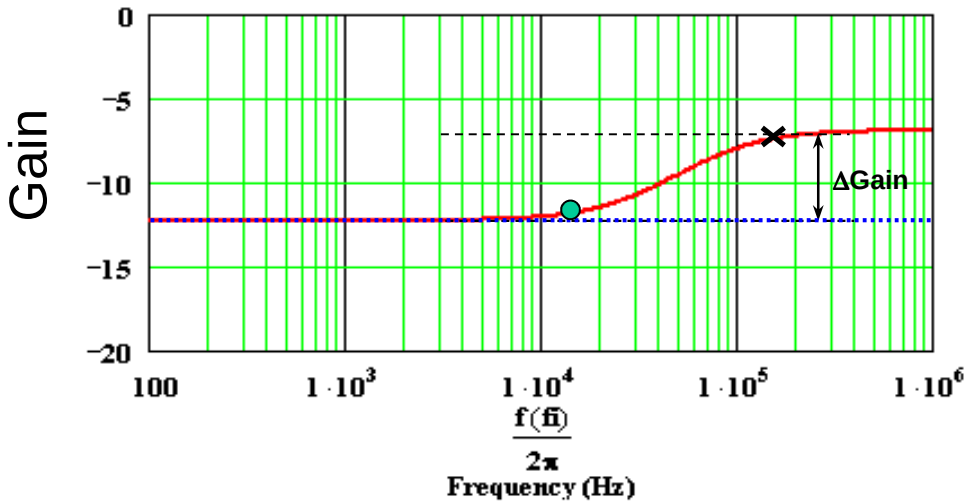
3. Choose optimum values of the resistor divider network $K_{REF}(s)$ and ITH compensation network A(s)

Feedback Voltage Divider and Phase Boost

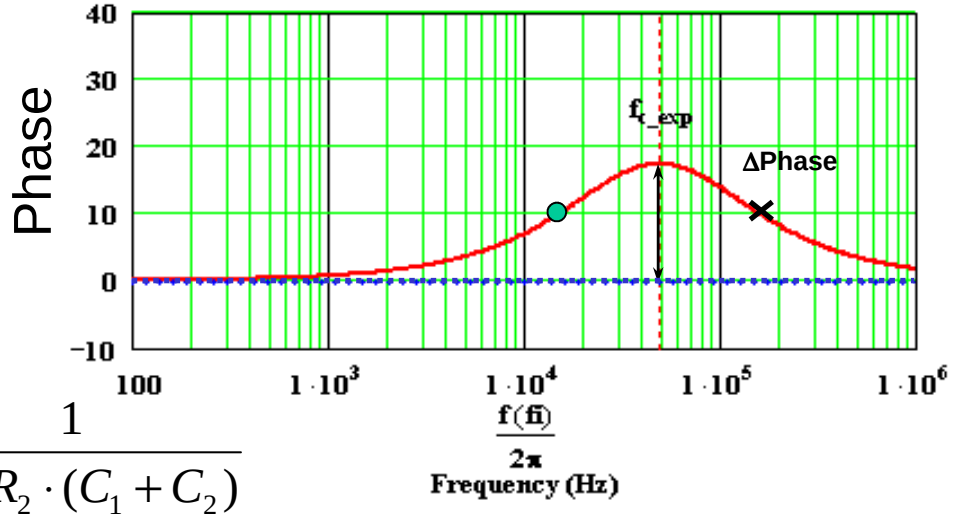


$K_{ref}(s)$

$$K_{REF} = \frac{V_{REF}}{V_o} = \frac{R_1}{R_1 + R_2}$$



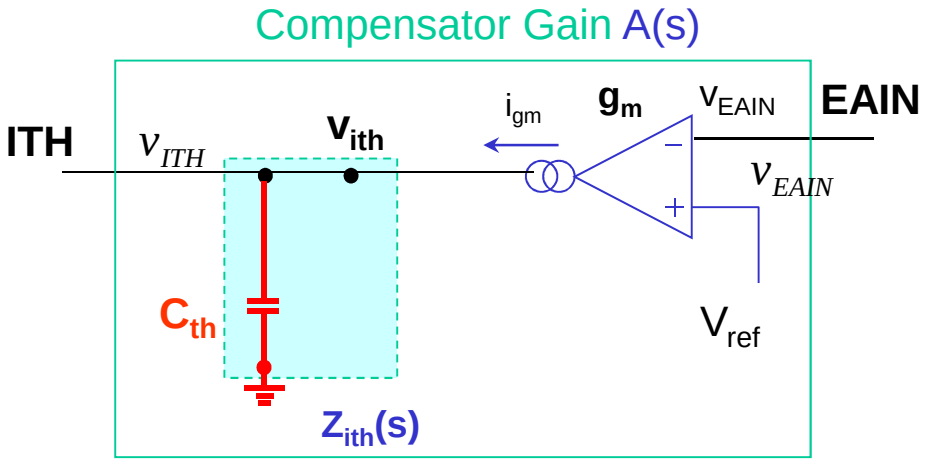
$$K_{REF}(s) = \frac{v_{EAIN}(s)}{v_o(s)} = K_{REF} \cdot \frac{1 + \frac{s}{2\pi \cdot f_{z\_ref}}}{1 + \frac{s}{2\pi \cdot f_{p\_ref}}}$$



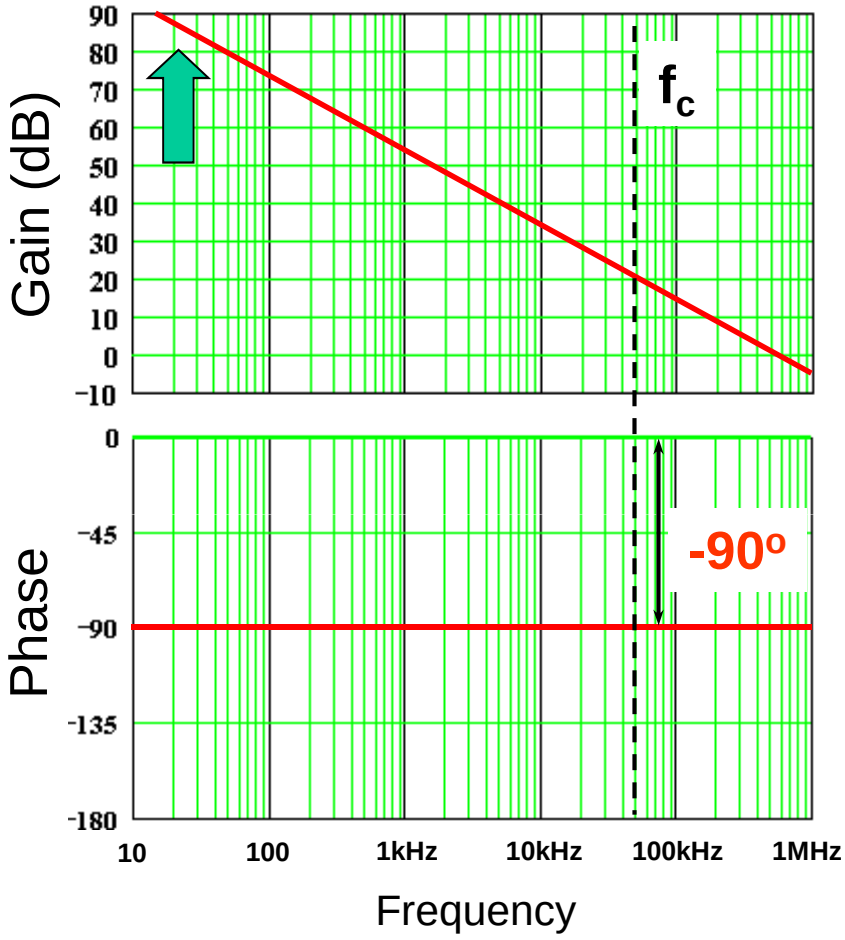
$$f_{z\_ref} = \frac{1}{2\pi \cdot R_2 \cdot C_2} \qquad f_{p\_ref} = \frac{1}{K_{REF}} \cdot \frac{1}{2\pi \cdot R_2 \cdot (C_1 + C_2)}$$

C_1 and C_2 provide phase boost around the cross-over frequency.

ITH Compensation – High DC Gain



$$A(s) = \frac{v_{ITH}(s)}{v_{EAIN}(s)} = -g_m \cdot (Z_{ith}(s))$$

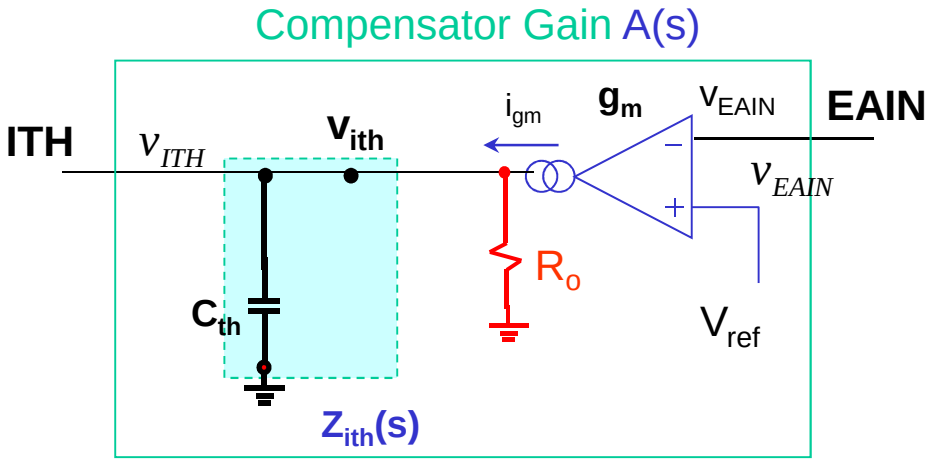


1. Simple Integrator:

$$A(s) = -g_m \cdot \frac{1}{C_{th} \cdot s}$$

- High low frequency gain for accurate DC Vout regulation
  - -90° phase delay @ expected cross-over frequency f_C

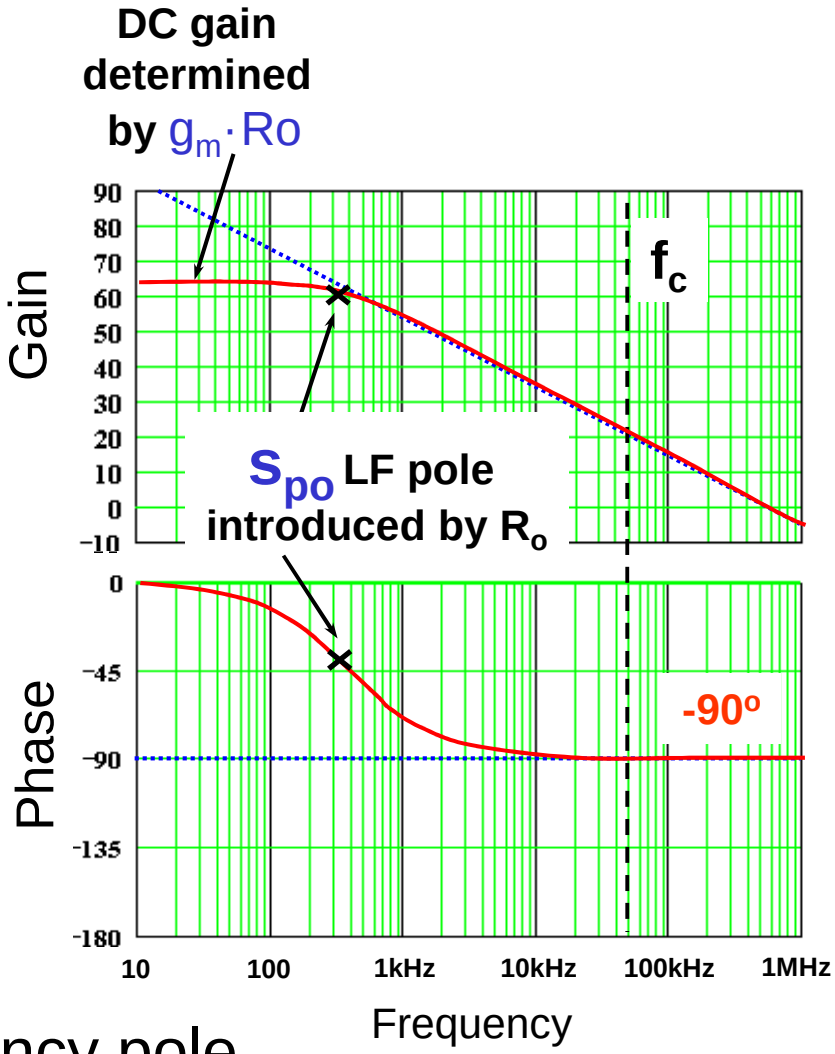
ITH Compensation – LF Pole



$$A(s) = \frac{v_{ITH}(s)}{v_{EAIN}(s)} = -g_m \cdot (Z_{ith}(s))$$

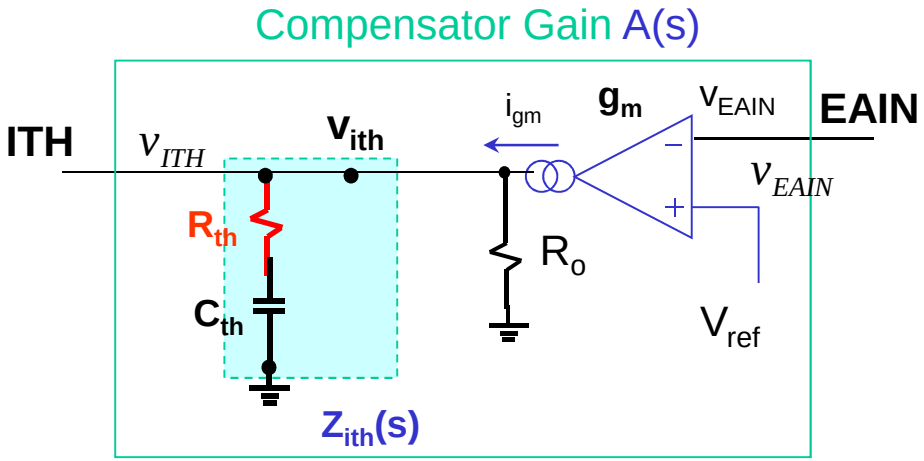
2. Simple Integrator with g_m Op-Amp Output Impedance R_o:

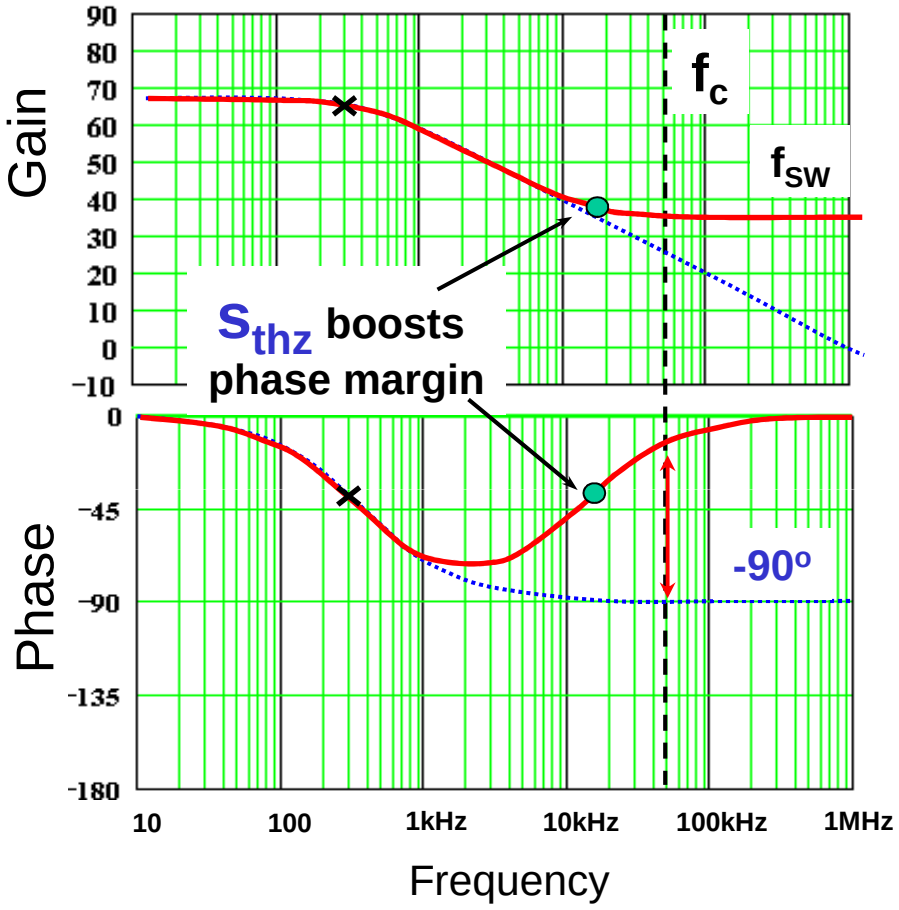
$$A(s) = -g_m \cdot R_o \cdot \frac{1}{(1 + \frac{s}{s_{po}})} \qquad s_{po} = \frac{1}{R_o \cdot C_{th}}$$



- g_m Op-Amp adds a low frequency pole
- Still -90° phase delay @ f_C

ITH Compensation – Add Zero for Phase





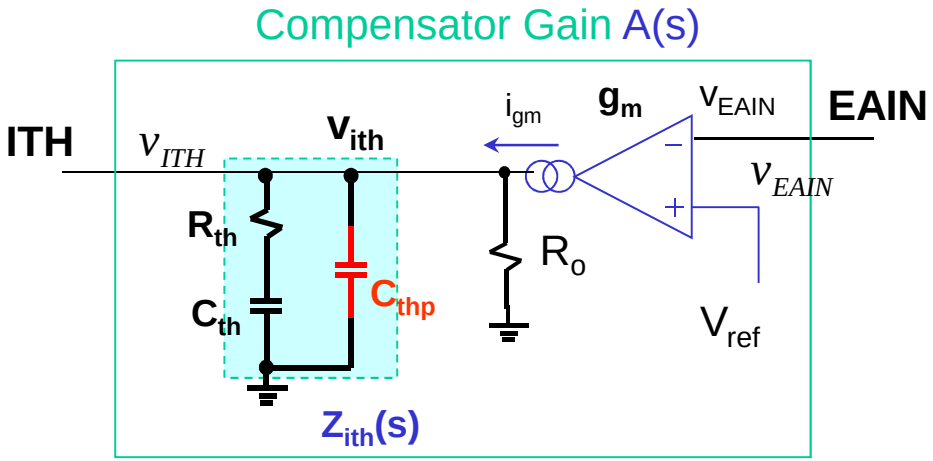
3. Add zero for Phase Compensation at cross over frequency:

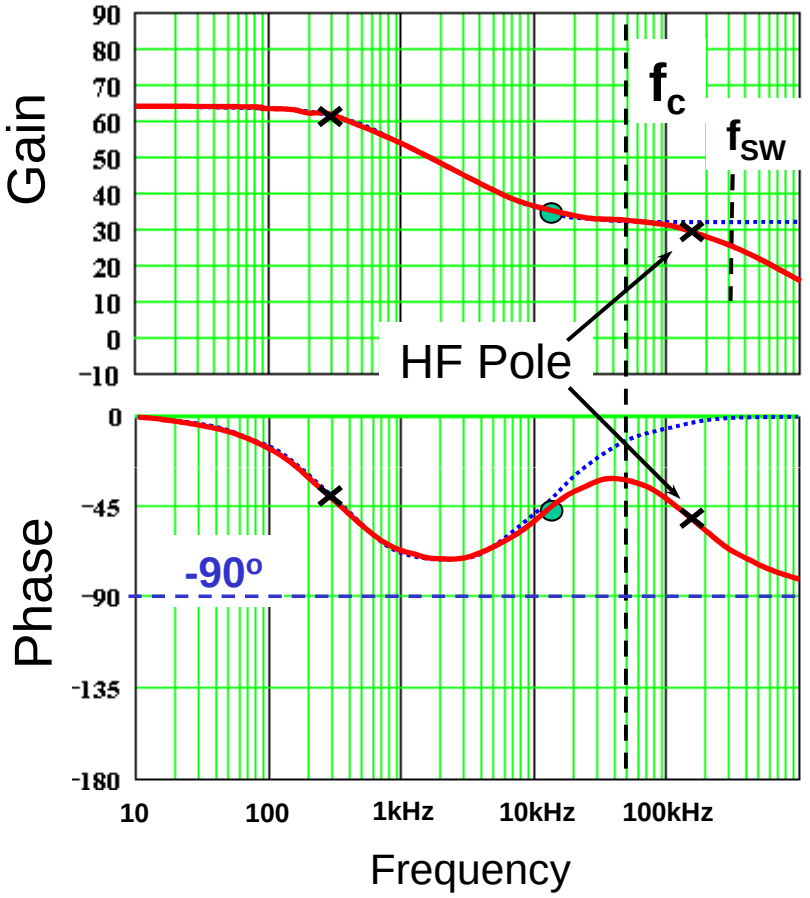
$$A(s) = -g_m \cdot R_o \cdot \frac{1 + \frac{s}{s_{thz}}}{(1 + \frac{s}{s_{po}})}$$

$$s_{thz} = \frac{1}{R_{th} \cdot C_{th}}$$

- Adds a zero before / around f_C to boost up phase
  - Increased gain @ high frequency

ITH Compensation – HF Pole





4. Add a high frequency pole to attenuate PCB switching noise:

$$A(s) = -g_m \cdot R_o \cdot \frac{1+\frac{s}{s_{thz}}}{(1+\frac{s}{s_{po}})\cdot(1+\frac{s}{s_{thp}})}$$

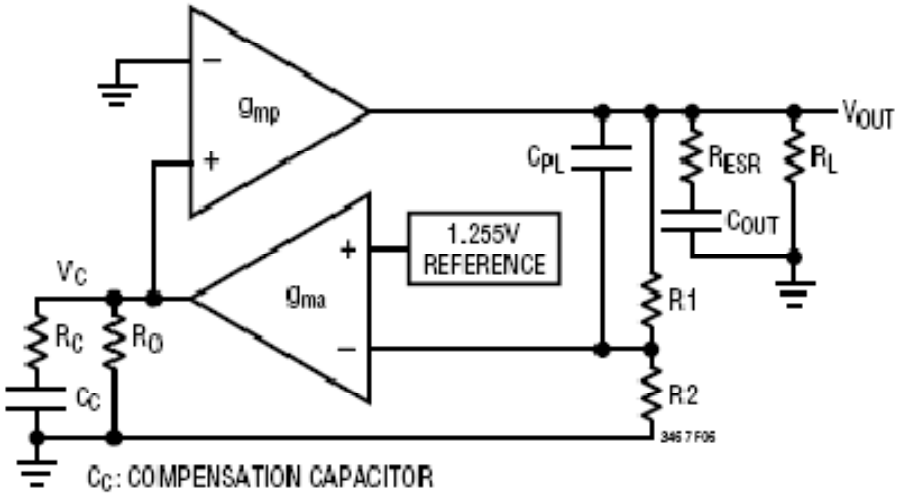
$$s_{thp} = \frac{C_{th}+C_{thp}}{R_{th}\cdot C_{th}\cdot C_{thp}} \approx \frac{1}{R_{th}\cdot C_{thp}} \quad \text{(Cth >> Cthp)}$$

How to define compensation network

Simulation :

- Use LTspice to generate Bode plot
- Check:
  - ➢ cross-over frequency (fc)
  - ➢ phase margin & gain margin (φm, Gm)
- Adjust compensation values

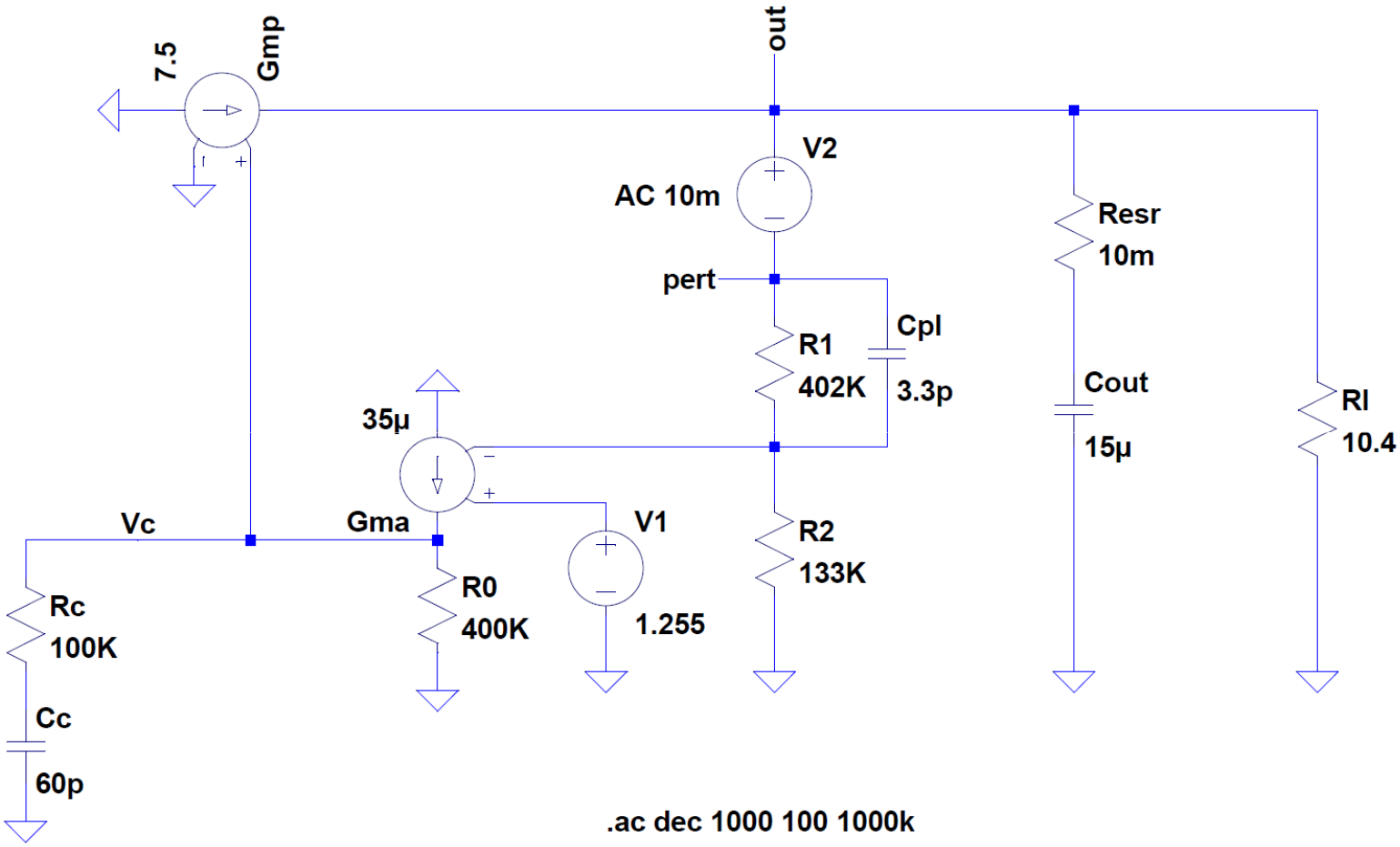
Extract from datasheet



CC: COMPENSATION CAPACITOR
COUT: OUTPUT CAPACITOR
CPL: PHASE LEAD CAPACITOR
gma: TRANSCONDUCTANCE AMPLIFIER INSIDE IC
gmp: POWER STAGE TRANSCONDUCTANCE AMPLIFIER
RC: COMPENSATION RESISTOR
RL: OUTPUT RESISTANCE DEFINED AS VOUT DIVIDED BY ILOAD(MAX)
RO: OUTPUT RESISTANCE OF gma
R1, R2: FEEDBACK RESISTOR DIVIDER NETWORK
RESR: OUTPUT CAPACITOR ESR

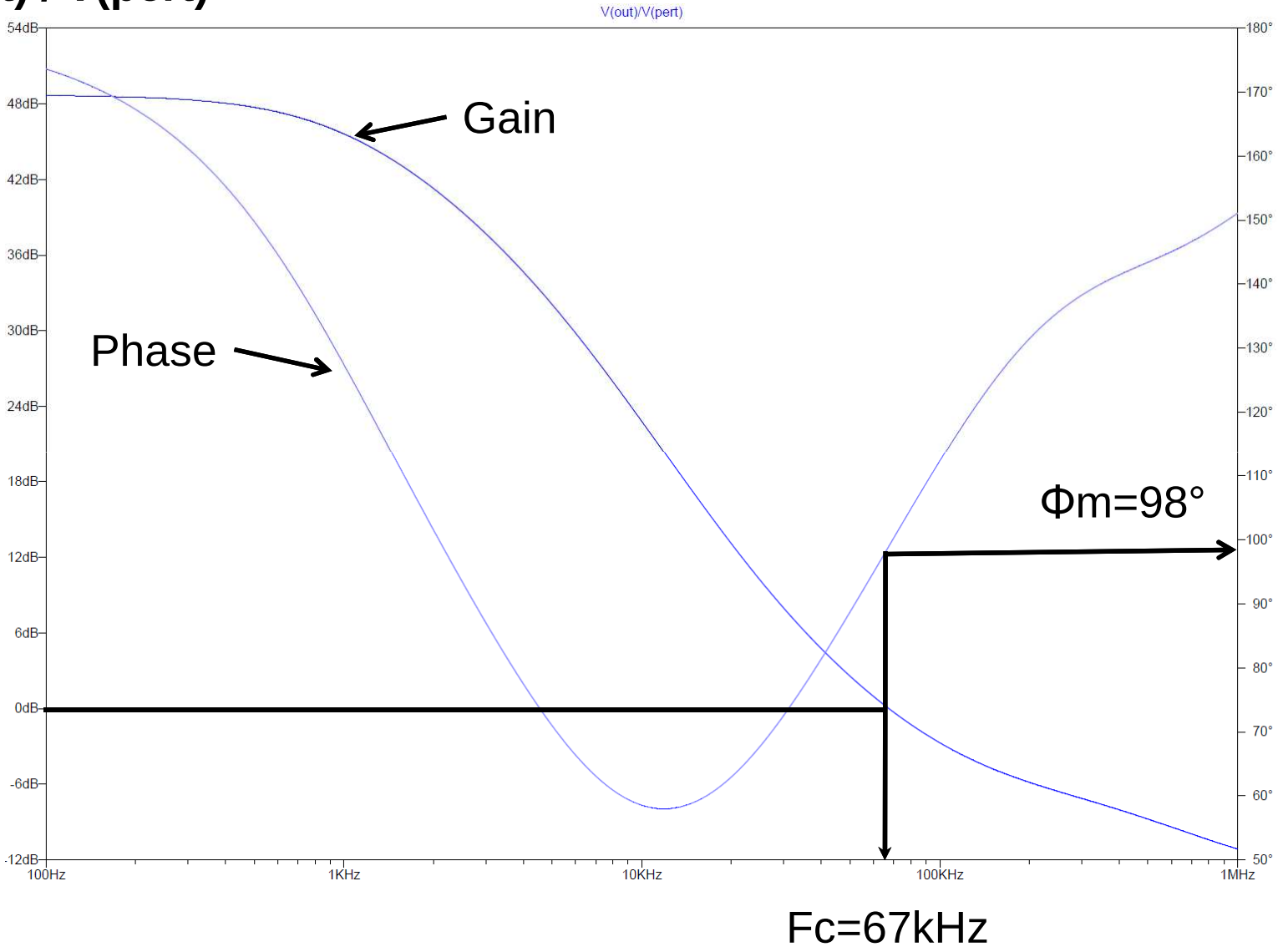
Parameter	Value	Units
R_L	10.4	Ω
C_{OUT}	15	µF
R_{ESR}	10	mΩ
R_O	0.4	MΩ
C_C	60	pF
C_{PL}	3.3	pF
R_C	100	kΩ
R1	402	kΩ
R2	133	kΩ
V_{OUT}	5	V
V_{IN}	3.3	V
g_{ma}	35	µmho
g_{mp}	7.5	mho
L	2.7	µH
f_S	1.3*	MHz

LTspice to generate Bode plot



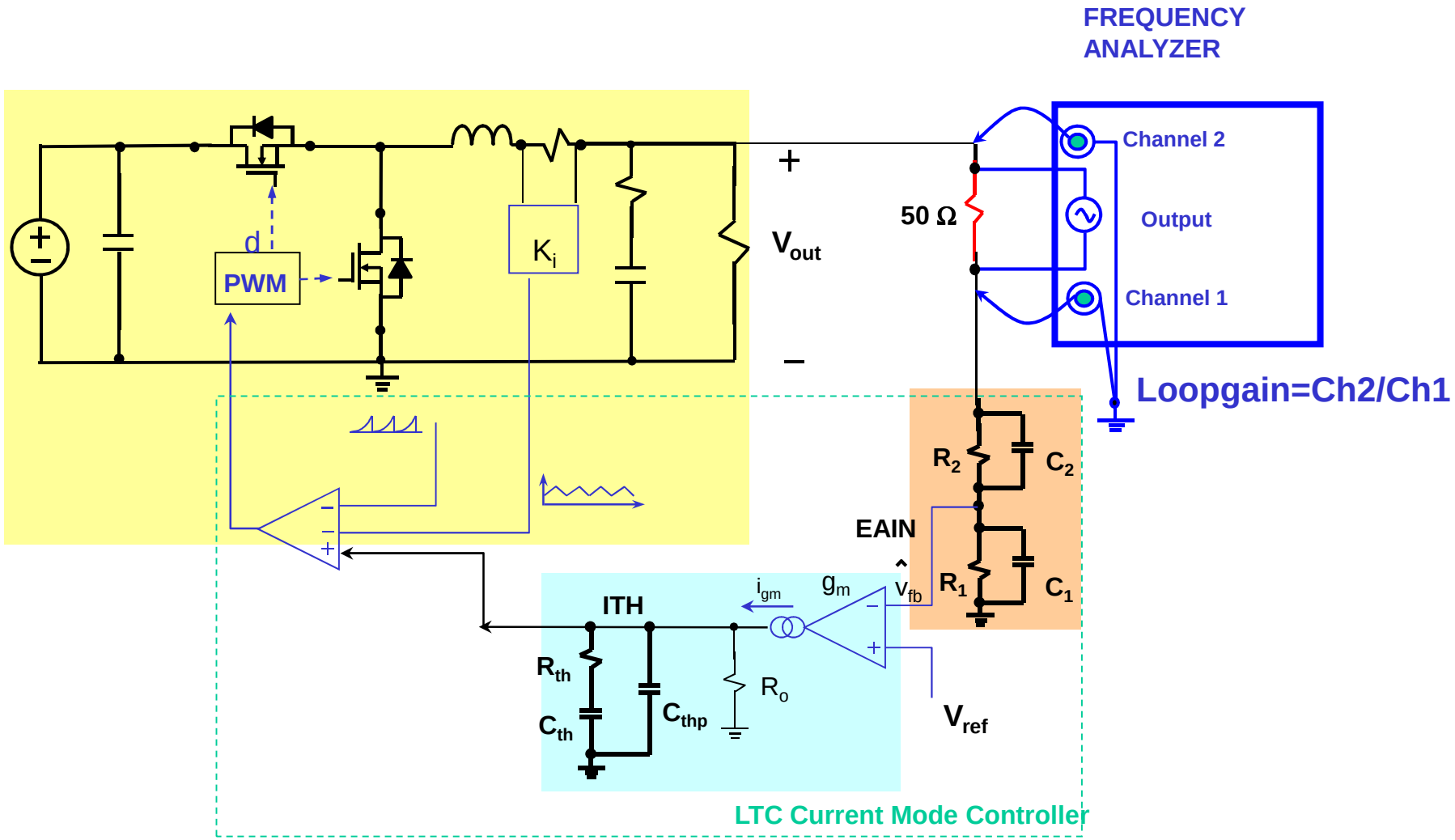
LTspice to generate Bode plot

V(out) / V(pert)



Practical Tests

Measure the Voltage Loop Gain



Typical Loop Gain and Phase Margin

LTC3729 Current Mode Buck Converter Typical Loop Gain